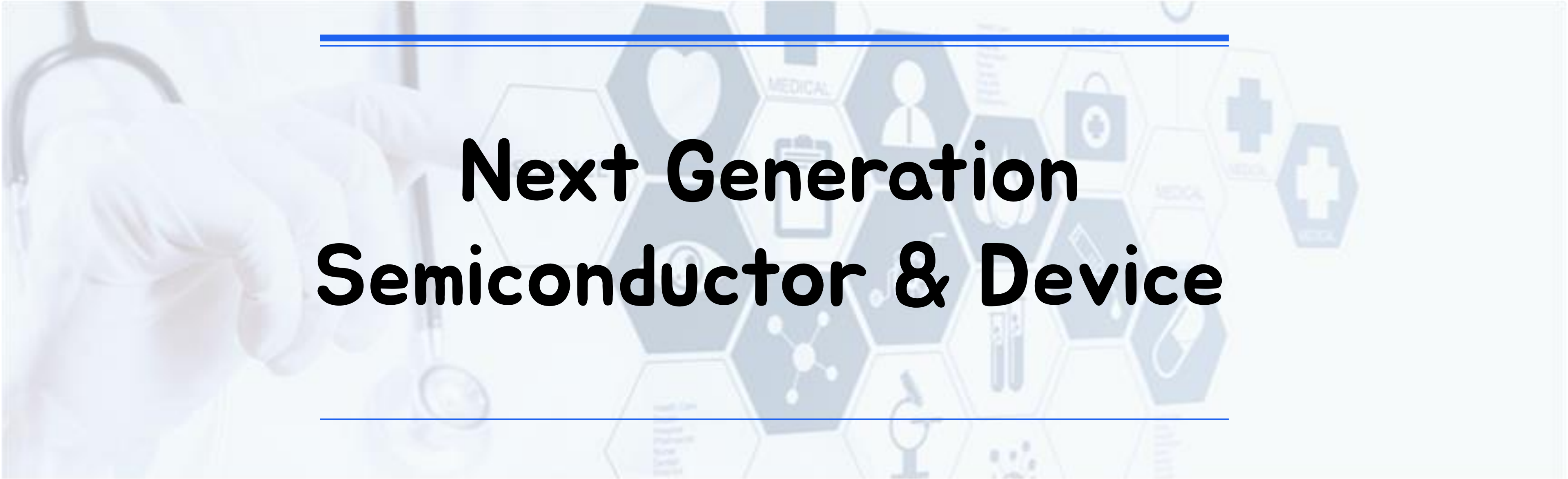
Solid State Physics Team Project



Next Generation Semiconductor & Device

3rd Team

문지원 김혜빈 선동훈 박규도

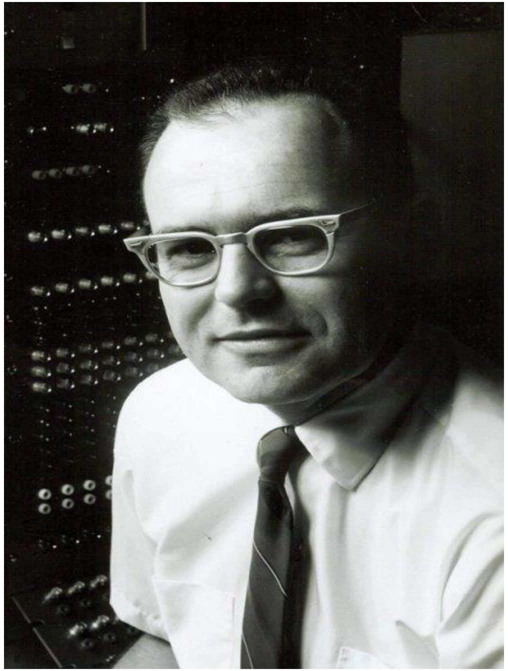
CONTENTS

Part 01. Introduction & Overview

MOON JIWON

01 Introduction &Overview

01 Introduction &Overview



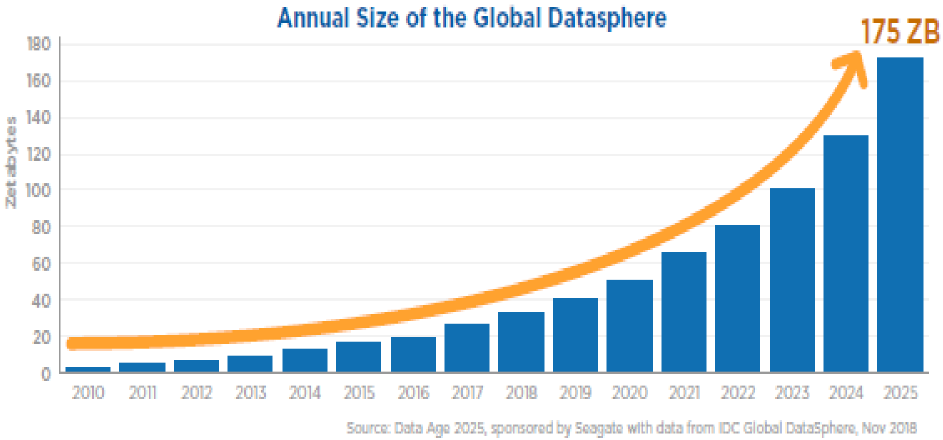
Gordon Moore – 'Moore　s Law'

Law on speed technology development.
Performance of semiconductor memory chips
is doubled from 18 months to 24 months.

01 Introduction & Overview

BUT, IN MODERN

physical limitations in process of refinement
flood of information



01 Introduction & Overview

'Requirements from s

Portability / networking

Top 3 functional elements of memory chips : density, non-volatility, speed

NEXT GENERATION

improving integration

accelerating operation

low power

01 Introduction & Overview

PRESENT - DRAM, Flash memory

DRAM

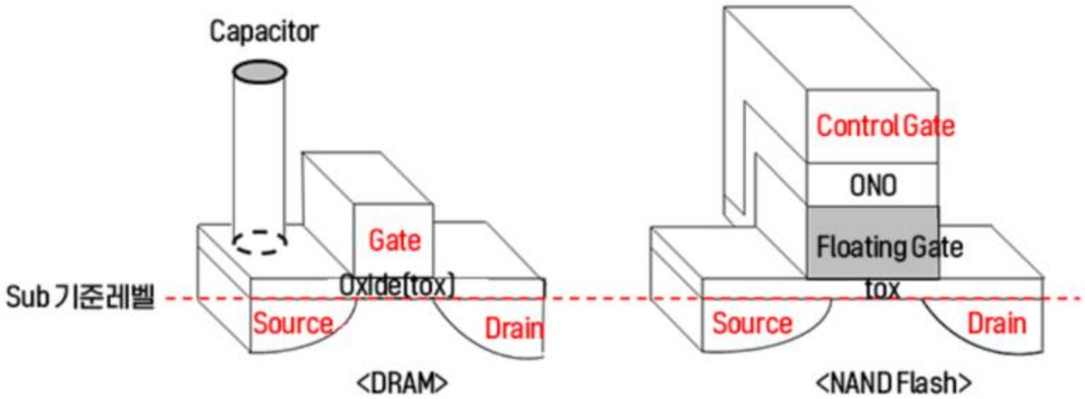
\+ small size, high speed

− volatile

Flash Memory

\+ nonvolatile

− speed, refinement

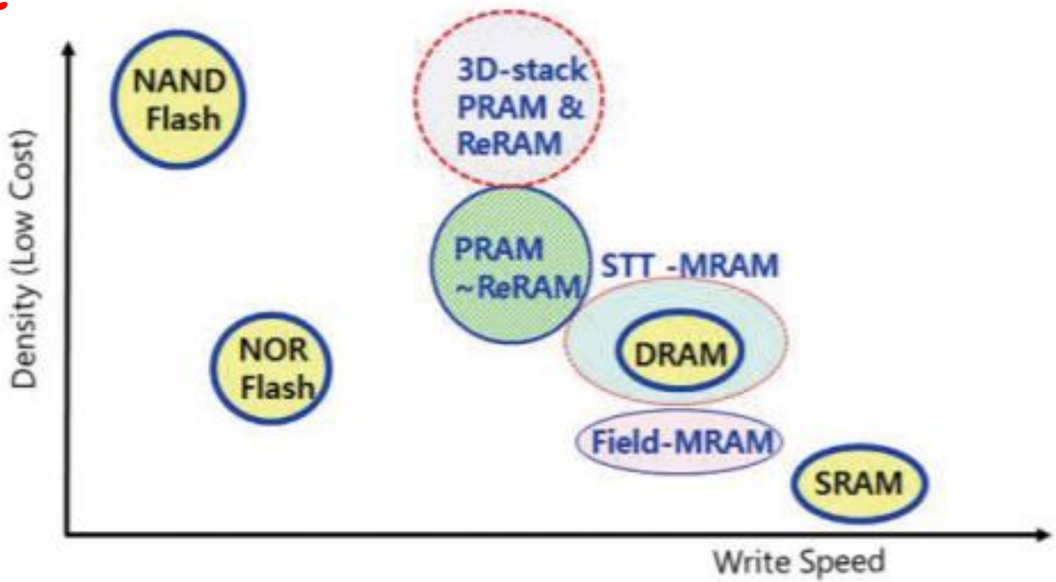


01 Introduction &Overview

	property	advantage
PRAM (Phase change RAM)	State change of materials	Fine line width
RRAM (Resistive RAM)	change in electrical resistance	Low voltage
MRAM (Magnetic RAM)	magnetic field	High speed Universal memory

01 Introduction &Overview

※reference

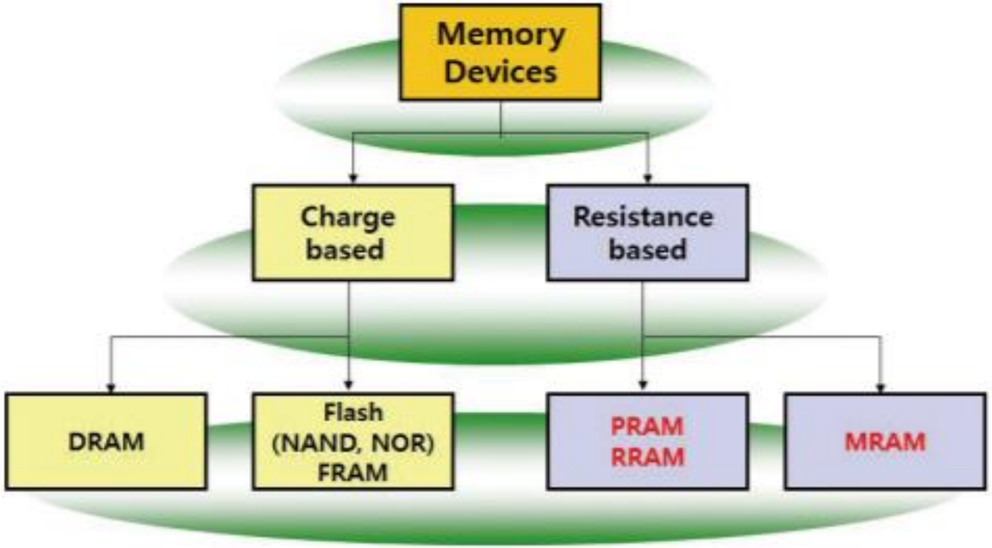


The comparison of existing and new memory devices

Part 02.
Theory

KIM HYEBIN

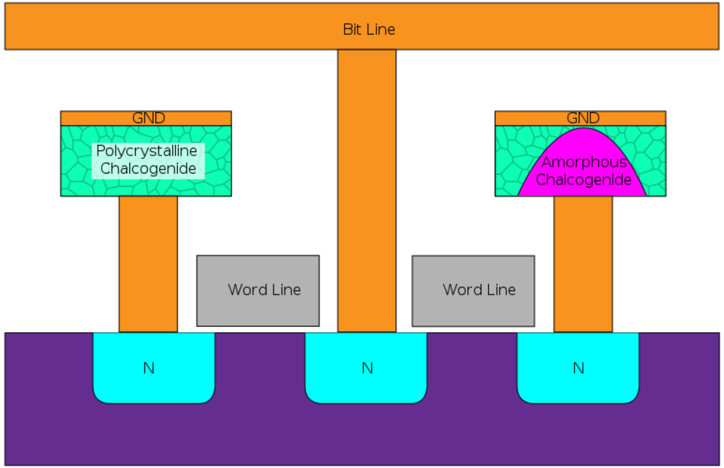
02 Theory



PRESENT **NEXT GENERATION**

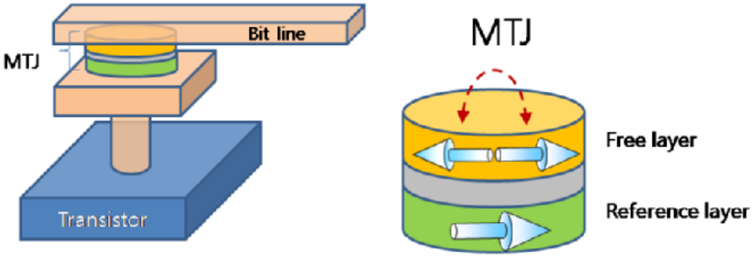
02 Theory <PRAM>

Mechanism of PRAM



- Current, voltage applied
- Occurred reversible phase changing between crystal(Low electrical resistance) &amorphous(High electrical resistance)
- Store information using resistance differences.

02 Theory <MRAM>



MRAM is a memory that have the unit cell, MTJ(Magnetic Tunnel Junction).
-MTJ based on resistance changing.

MRAM
has the Shrink Limitation!!

Shrink : The operation of reducing a designed chip to a constant ratio depending on the process conditions.

02 Theory 〈MRAM〉

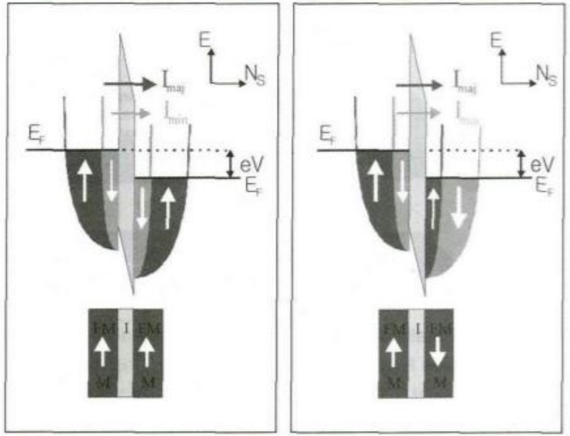


Fig. 3. Energy band structures and spin-polarized electron tunneling for parallel and antiparallel configurations of magnetizations in a magnetic tunneling junction.

Spin direction

Parallel
-tunneling , resistance

Antiparallel
-tunneling , resistance

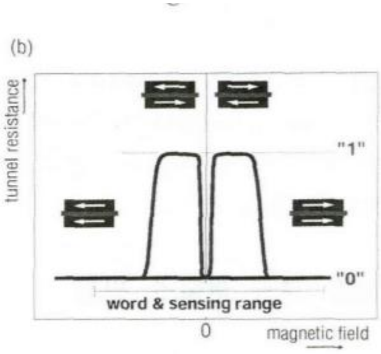


Fig. 6. (a) Structure of MRAM module consisting of a magnetic cell and two conducting wires, and (b) R-H curve of a magnetic tunneling junction.

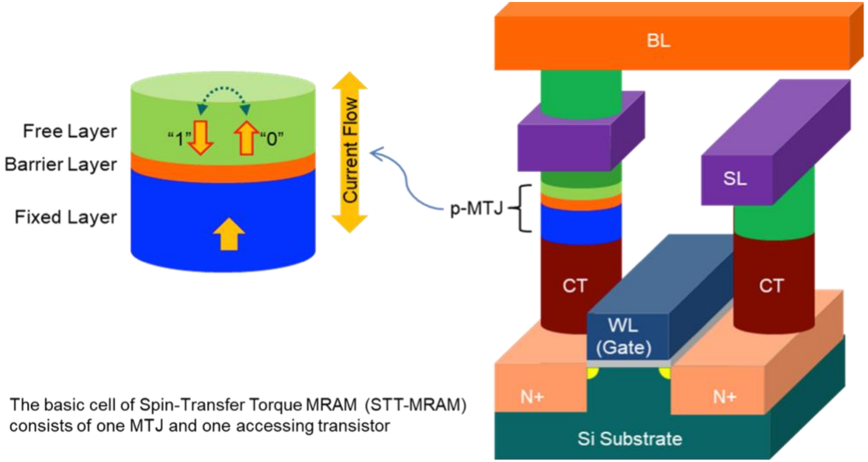
MRAM
has the Shrink Limitation!!

Shrink : The operation of reducing a designed chip to a constant ratio depending on the process conditions.

02 Theory <STT-MRAM>

STT-MRAM (Spin-Transfer-Torque Magnetoresistive Random Access Memory)

STT : The physical phenomenon that we can control the spin direction of magnetic material when we inject current or voltage.

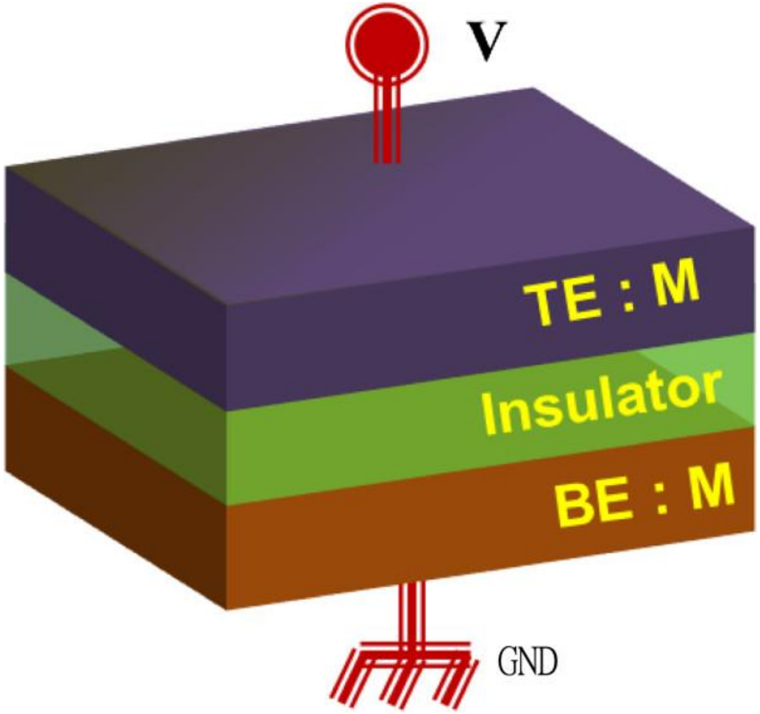


The basic cell of Spin-Transfer Torque MRAM (STT-MRAM) consists of one MTJ and one accessing transistor

Mechanism of STT-MRAM

-Injecting Voltage or Current
-Transport the spin from electron to magnetic material
-Control the direction of spin

02 Theory 〈RRAM〉



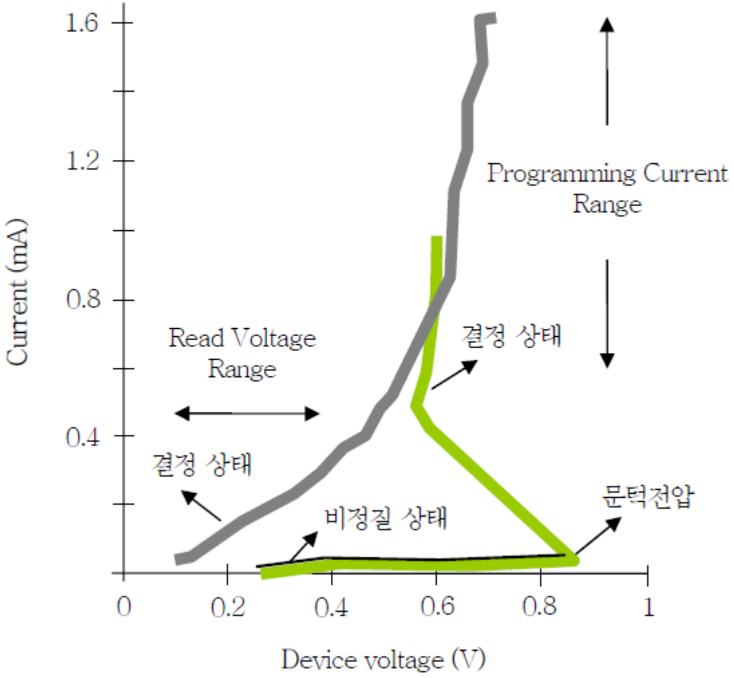
Mechanism of RRAM

- the insulator between two electrode has a large resistance
- Injecting Voltage
- forming filament
- electron flows(lower resistance)

Part 03. Experiment

SUN DONGHOON

03 Experiment <Voltage-Current>



Crystallized set state

- Similar as metal

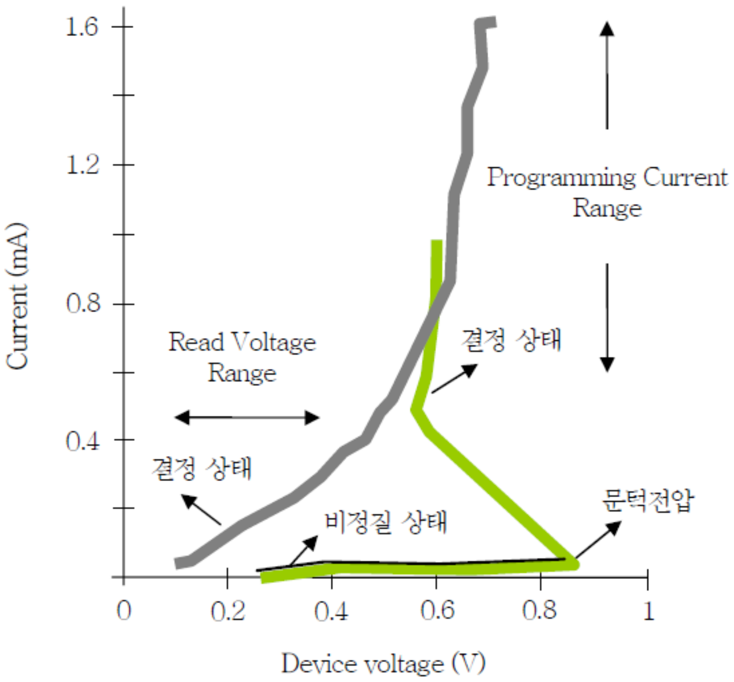
Amorphous reset state

- High resistance
- Over the threshold voltage characteristic reversed

Grey line : crystallized set state

Green line : amorphous reset state

03 Experiment <Voltage-Current>



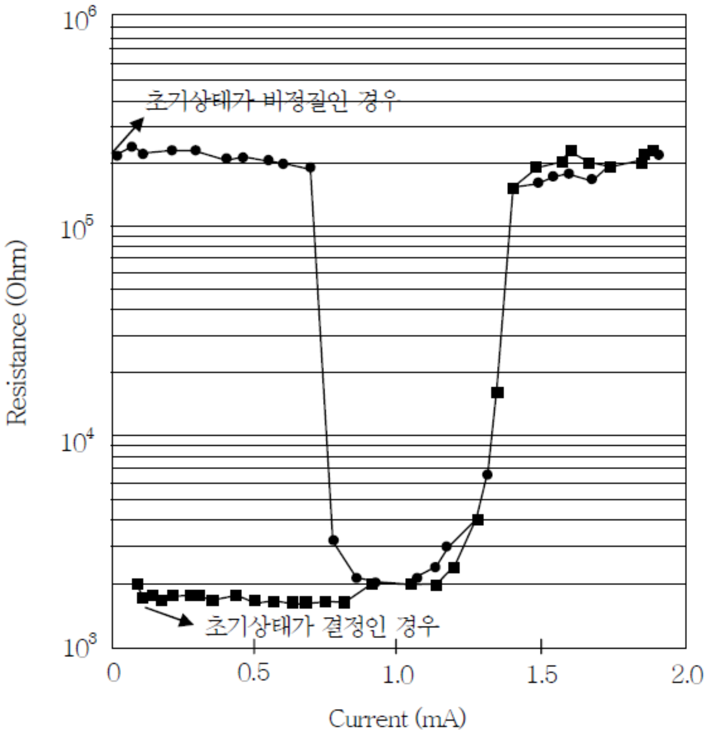
Make voltage 0.4V

Do not cause phase change by reading

Grey line : crystallized set state

Green line : amorphous reset state

03 Experiment <Current-Resistance>



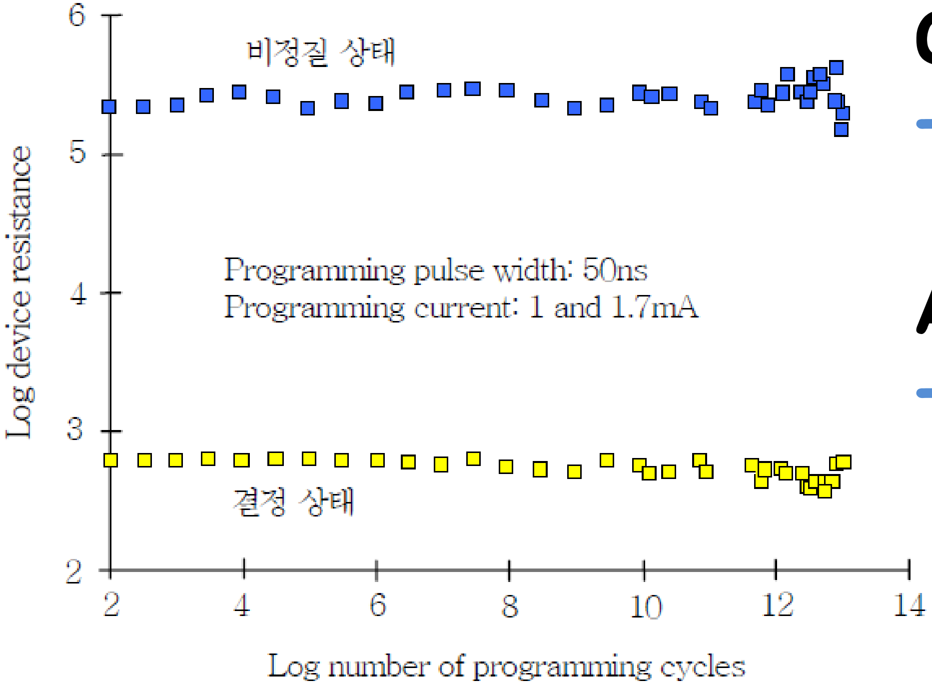
Crystallized state

- Change to amorphous state

Amorphous state

- Change to crystallized state
  Change to amorphous state again

03 Experiment <Voltage-Current>



Crystallized set state

- resistance lower than 1 k

Amorphous reset state

- resistance about 100 k

Yellow line : crystallized set state

Blue line : amorphous reset state

Part 04.
Application

PARK KYUDO

04 Application of PRAM

Advantages of PRAM

- Smaller
- Faster
- More reliable
- More mass-produced

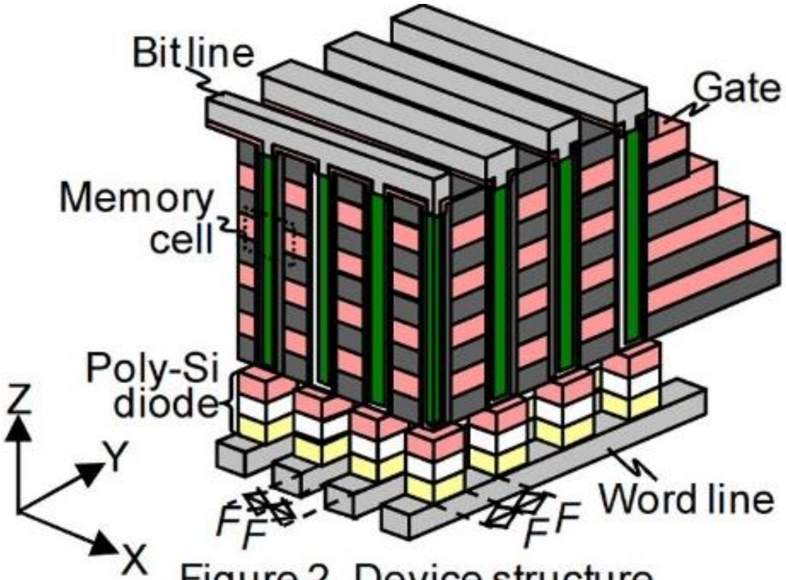


Figure 2. Device structure of VCCPCM array

04 Application of PRAM

Stable in high temperature

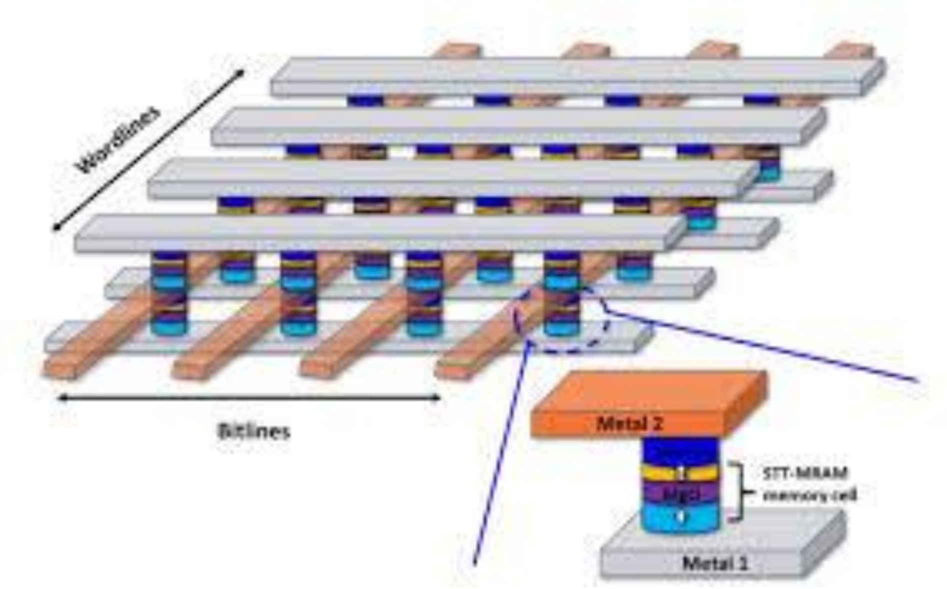
- useful for mobile device memory

Time to store data would greatly reduce

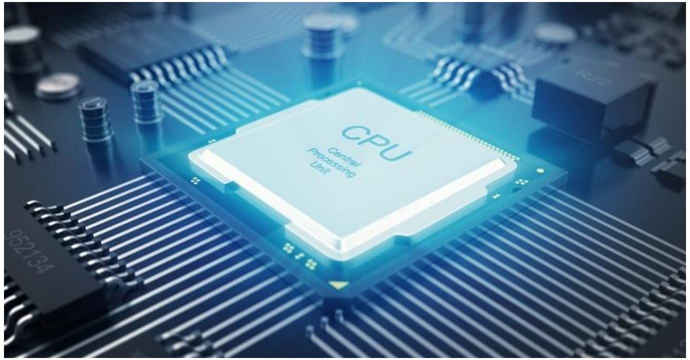
04 Application of MRAM

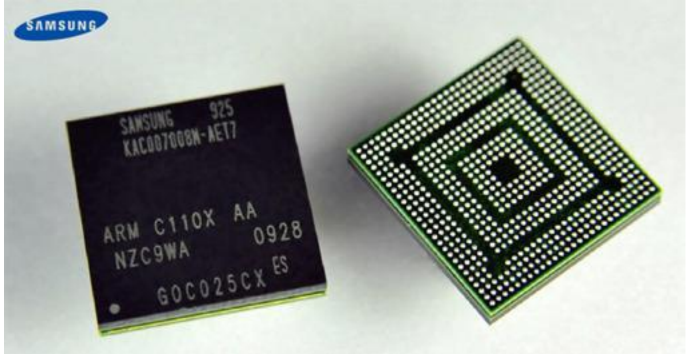
Advantages of MRAM

- Fast speed
- High capacity
- High density



04 Application of MRAM



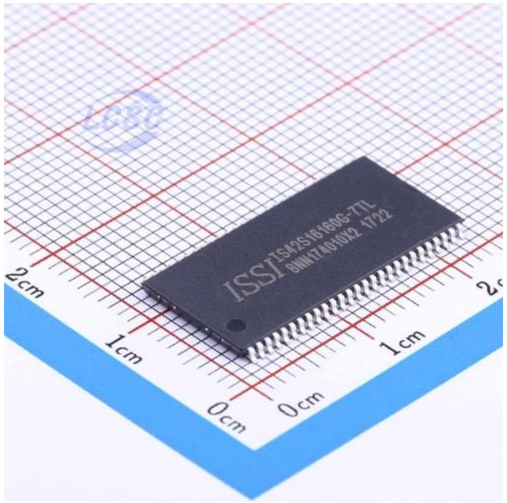


04 Application of RRAM

Advantages of RRAM

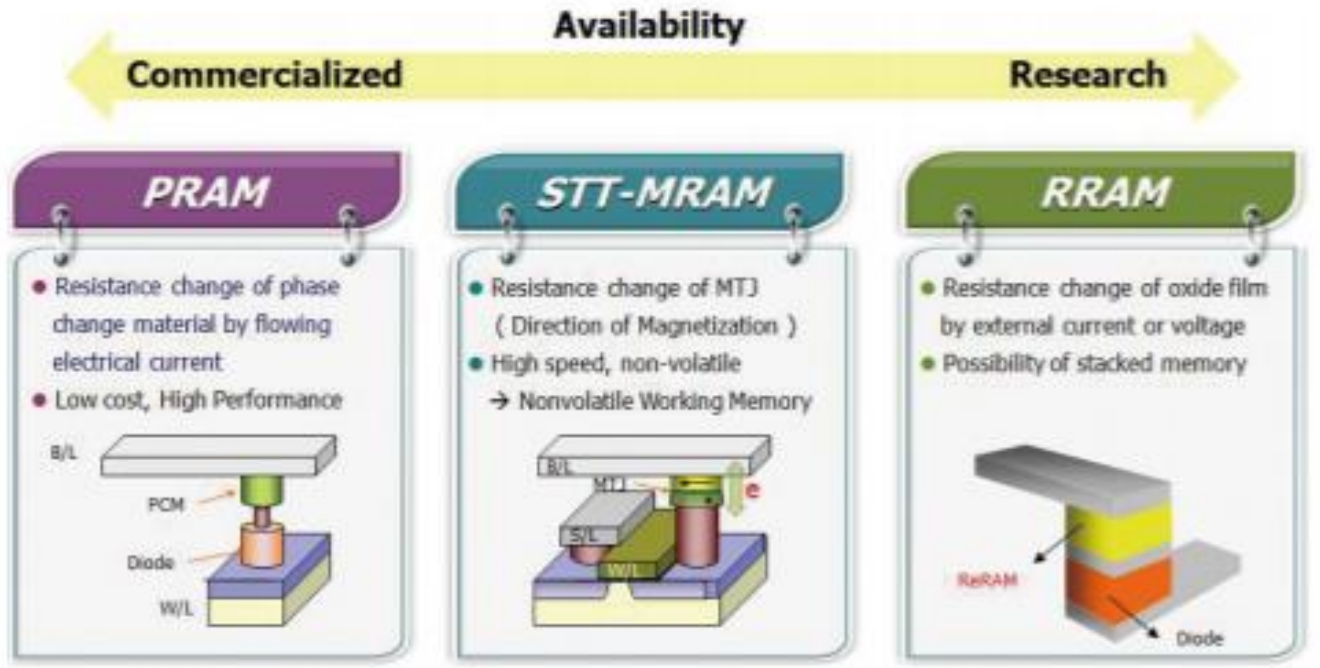
- Improving integration
- Storing large quantities with low power
  -> make memory smaller
- Semipermanent

04 Application of RRAM



Miniaturized memory -> larger capacity of electronic devices

04 Application



05 References

[1] David Reinsel-John Gantz-John Rydning.(2018). The Digitization of the world from edge to core. IDC
[2] 백승재, 이붕주, 박구범. (2011). 반도체 뉴메모리의 동향 및 전망. 전기의세계, 60(1), 34-39.
[3] 이희덕. (2015). 차세대 반도체 소자 기술. 전자공학회지, 42(7), 17-17.
[4] J. H. Jang, et al.,' Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultrahigh density NAND flash memory', 2009
[5] The Prospect of the Phase-change Access Memory Technology, 박영삼 외 2명, 기능성전자소자팀, 전자통신동향분석 제 20권 제 6호, 2005
[6] Development Status and Prospect of New Memory, Hongsik Jeong, 반도체 소자 및 공정기술 특집
[7] 김찬경. (2019). 삼성전자 Foundry 사업부 탐방 차세대 메모리 : STT-MRAM. 정보과학회지, 37(6), 60-62.
[8] 지수영, 정성우. (2010). PRAM 을 이용한 고성능 SSD 연구. 한국통신학회 학술대회논문집, (), 1717-1718.
[9]MRAM 최근 기술 동향, 이우영, 신경호(한국과학기술연구원 박막기술연구센터), 김창경,이지현(한양대학교 재료공학부, 세라미스트, 제 4권 제 2호, (2001)

Thank you for listening